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# Discussing Multiple Topologies for Mitigating THD of Load Voltage Profile

Sameer Bhambri[a*], Vivek Shrivastava[b], Manoj Kumawat[c]

## ABSTRACT

In traditional power systems, power quality is defined as the quality of voltages as supplies are voltage sources rather than current sources. In the renewable energy based power systems, inverters and loads/grid are two major sources of harmonics. This paper provides the comprehensive working mechanism and performance comparison of four different strategies, discussed and applied for reducing the $\mathrm{THD_V}$ (voltage total harmonic distortion) of output voltage. The strategies, which are BHCC (Bypassing harmonic current components), HDC (harmonic droop control), integral controller and resonant impedance are discussed thoroughly and applied to the robust droop control model of single phase inverters operating in parallel. The modification in the BHCC strategy is incorporated in order to further enhance the output voltage quality that led $\mathrm{THD_V} < 5$ %. The FFT (fast fourier transform) analysis of output voltage is carried out for aforementioned strategies to evaluate the $\mathrm{THD}$ reduction in the output voltage. Matlab/Simulink tool is used to validate the proposed strategies for nonlinear load.

**Keywords:** $\mathrm{THD}$, Droop, Robust, Harmonic, Renewable energy based power systems

## Abbreviations:

PQ: power quality; PWM: pulse width modulation; $\mathrm{THD}$: total harmonic distortion; $\mathrm{THD_V}$: voltage total harmonic distortion; $\mathrm{Z_0}$: output impedance

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***Corresponding Author:**

[a,c]*Electrical Engineering,*
*National Institute of Technology*
*Delhi*
*Email: sameerbhambri@nitdelhi.ac.in*

[b]*Electrical Engineering,*
*National Institute of Technology*
*Uttrakhand*

## I. INTRODUCTION

Degradation in the PQ can be discussed in many ways, e.g., variations in frequency and magnitude, poor power factor, phase imbalancing, harmonics in the waveform etc. Some well known power quality terms are shown in the Table1. There are multiple reasons which are responsible for the power quality problem (Wakileh, 2001). Nowadays, use of distributed generation and renewable energy sources, e.g., solar, wind, tidal etc trends across the globe (Bhambri, Shrivastava, et al., 2023). They commonly use power inverters to build microgrids, which may or may not be grid-connected. The presence of harmonics in load/output voltage, caused by switching phenomena of inverters, is a serious concern in these applications (Zhong, 2011).

**Table 1** Terms described in power quality

| Terms | Interpretation |
|---|---|
| **swell** | RMS quantity > the nominal value by 10% - 80% for half cycle – 1 min |
| **dip** | RMS quantity is < the nominal value by 10% - 90 % for half cycle – 1 min |
| **flicker** | repetitive or random variations in the root mean square value of voltage between 0.9 p.u and 1.1 p.u of nominal value. |
| **impulses** | brief abrupt increment in the voltage. |
| **under-voltage** | voltage drops < 0.9 p.u of nominal value for more than a minute |
| **over-voltage** | voltage rise > 1.1 p.u of nominal value for more than a minute |
| **harmonics** | Distorted waveshape of quantity. |

There are primarily more than one sources of harmonics: one is through the inverters (due to the PWM and switching) and the other is through the loads or the grid. When a pure sinusoidal voltage is applied to nonlinear loads, harmonic currents are generated. The harmonic currents then produce harmonic voltage components as a result of impedances in the distributed network as well as inside the supply sources. Of course, harmonic voltages generate harmonic currents as well. Triplen harmonics are the odd multiples of the third harmonic (3rd, 9th, 15th, 21st, etc.), sometimes known as (6n-3) order harmonics. These currents in a 3-φ system are zero sequence harmonics that add in the neutral line and are of special importance. The (6n-1) order harmonics are negative (-) sequence harmonics, which are problematic for rotating machines because these cause negative (-) torque and attempt to drive machine in the opposite direction. The presence of harmonics is not prudent because these cause increased losses, overheating, distorted current and voltage waveform, decreased capacity etc. Therefore it has become a major concern in the modern power system. As per the IEEE-519 standard, the THD of output bus voltage and line current (exchanged with grid) requires to be maintained below 5% (Zhong & Hornik, 2012a).

A realistic approach is to use regulators, and as a result, numerous feedback control systems are available to lower the voltage total harmonic distortion of inverters (Cheepati et al., 2025). This is mostly a tracking issue with a sinusoidal reference that rejects other additional harmonic components. Hysteresis controllers are one such example. Repetitive control theory, a simple learning control approach, can handle a large number of harmonics at the same time since it has a high gain at the fundamental and all other frequencies. It has been applied successfully to constant-frequency-constant-voltage PWM inverters, grid tied inverters and active filters (Hara et al., 1988). The literature pertaining to power quality in power systems reports strategies that have been developed to reduce THD in the grid current, system voltage and both grid current and the system voltage (Hornik & Zhong, 2010; Zhong & Hornik, 2012b). The cooperation among distributed inverters to evenly share harmonic VAr results in low THD (Lee et al, 2007).

Another approach is to investigate the voltage degradation mechanism in order to identify ways for addressing power quality issues. The output impedance, $Z_0$ of the inverter plays a vital role in minimizing the THD of the load voltage. The THD can be reduced by lowering the output impedance at the dominant harmonic frequency components (Zhong & Zeng, 2016). This can be accomplished by designing a feedback integral controller that causes, $Z_0$ the output impedance of an inverter to be capacitive in nature. An integrator constant is meant to address both the third and fifth harmonic components in the output voltage (Zhong & Zeng, 2013; Zhong & Zeng, 2011). The limitations of

conventional droop control are overcome by robust droop control model for a 1-φ resistive inverter (Bhambri, Kumawat, et al., 2023). In addition, Bhambri et al. (2024) designs capacitive virtual impedance loop besides tuned inner controllers for reducing the load voltage THD. One of the recent works on interaction between grid connected inverters and grid background harmonics is reported by Tao et al. (2024), resulting in additional frequency components in network.

Although, there are number of literatures relating to the harmonic reduction in the power systems, still the mechanism of reducing the $\mathrm{THD_V}$ in the output voltage through different methods are not discussed at the same place in a comprehensive manner. Apart from this the concept of bypassing the harmonic currents is modified further to reduce the $\mathrm{THD_V}$ below 5% as per the IEEE-519 standard. Conjunctively, the model for proportional load sharing by parallel operating inverters and its importance is cited in the paper. Keeping this in mind, the following objective is set and achieved in the paper.

1. To introduce and evaluate different strategies for reduction in THD of output voltage.

The organization of paper is as follows, Section-II introduces the degradation mechanism of load voltage. Section-III provides thorough discussion of four different strategies to reduce THD of output voltage. Section -IV discusses results in form of simulation and FFT analysis. Section-V concludes the paper.

## II. DETERIORATION MECHANISM OF VOLTAGE

Various renewable energy sources, such as tidal, wind and solar power are increasingly being developed (Bhambri, Shrivastava, et al., 2023). Microgrids are commonly formed using power inverters, which may or may not be connected to the grid. Degradation in the voltage supplied by inverters is a significant PQ issue in these applications, especially under nonlinear load (Zhong, 2011).

The output voltage ($\mathrm{v_0}$) of such an inverter, modelled in Fig.1 is described in (1).

$$\mathrm{v_o} = \mathrm{v_r} - i \cdot \mathrm{Z_o(s)} \tag{1}$$

The current $i$ contains harmonics due to the inclusion of nonlinear load or/and the PWM in the inverter thus causing harmonic voltage drop in the impedance, $\mathrm{Z_0}$. Harmonic voltage components appearing in the output voltage will degrade the output voltage and induces total harmonic distortion (THD). THD may also appear in the output voltage due to harmonic components in the voltage reference, $\mathrm{v_r}$. One possible solution to make output voltage harmonic free, is to keep the reference voltage clean. Additionally, magnitude of inverter output impedance should be as small as possible over the frequency range of dominant harmonic frequency components. Another way is to deroute harmonic current components present in current $i$, in order to make it clean. In the third option, the reference voltage ($\mathrm{v_r}$) should provide the adequate amount of harmonic voltages ($\mathrm{v_{oh}}$) to neutralize the harmonic voltage drops in the output impedance, $\mathrm{Z_0}$.

### *A. Impact of inverter $\mathrm{Z_0}$*

The inverter current $i$ and its harmonic components can be written as

$$i = \sqrt{2}\sum_{h=1}^{\infty}\sin\left(h\omega t + \Phi_{\mathrm{h}}\right).\ \mathrm{I_h} \tag{2}$$

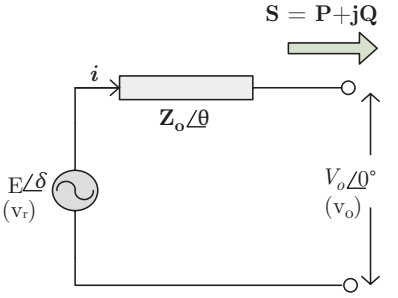



**Figure 1** Inverter Model

where E (volt) and δ (radians) are magnitude and phase angle of the reference voltage $\mathrm{v_r}$ ; $\mathrm{Z_0}$ (Ω) and θ (radians) are magnitude and angle of inverter output impedance; S, P and Q are apparent, active and reactive power; $V_0$ (volt) is voltage of output terminals and $i$ (amp) is current flowing through $\mathrm{Z_0}$.

The fundamental component of $\mathrm{v_0}$ is-

$$\mathrm{v_{o1}} = \mathrm{v_r} - \sqrt{2}\,\mathrm{I_1}\left|\mathrm{Z_o}\left(\mathrm{j}\omega\right)\right|\sin\left(\omega t + \Phi_1 + \theta\right) \tag{3}$$

assuming that the voltage reference ($\mathrm{v_r}$) is clean which is expressed as -

where

$$\mathrm{v_r} = \sqrt{2}\,\mathrm{E}\,\sin\left(\omega t + \delta\right) \tag{4}$$

$$v_{o1} = \sqrt{2}\, V_1 \sin\left(\omega t + \beta_o\right) \quad (5)$$

Where

$$V_1 = \sqrt{\left(E^2 + I_1^2 |Z_o(j\omega)|^2 - 2\, E\, I_1 |Z_o(j\omega)| \cos\left(\Phi_1 + \theta - \delta\right)\right)} \quad (6)$$

and

$$\beta_o = \tan^{-1}\left(\frac{I_1 |Z_o(j\omega)| \sin(\Phi_1 + \theta - \delta)}{I_1 |Z_o(j\omega)| \cos(\Phi_1 + \theta - \delta) - E}\right) \quad (7)$$

Now the harmonic components of the output voltage would be-

$$v_{oh} = \sqrt{2} \sum_{h=2}^{\infty} I_h \left|Z_o\left(jh\omega\right)\right| \sin\left(h\omega t + \Phi_h + \angle Z_o\left(jh\omega\right)\right) \quad (8)$$

By referring (8), it is clear that $v_{oh}$ depends upon impedance at harmonic frequencies and harmonic current components. $v_{o1}$ is determined by fundamental current, reference voltage and output impedance at fundamental frequency. This statement proves that $v_{oh}$ is not affected by $v_{o1}$ and this feature can be used to design the output impedance for different purposes. The $Z_0$ at harmonic frequencies can be reduced for an optimum value of capacitance, connected in series with filter inductor, in order to reduce the $THD_V$, expressed in (9). On the other hand, proportional load sharing of inverters is governed by output impedance at fundamental frequency and achieved through robust droop control model of 1-φ inverters (Zhong & Hornik, 2012a; Cheepati et al., 2025).

$$THD_V = \frac{\sqrt{\sum_{h=2}^{\infty} \left|Z_o\left(jh\omega\right)\right|^2 I_h^2}}{V_1} \quad (9)$$

## III. MECHANISMS FOR REDUCING LOAD VOLTAGE THD

### *A. Designing integrator constant (Integral controller)*

The objective of designing the capacitive type inverter is to reduce the output impedance at dominating harmonic components ($h$ = 3, 5..), thereby reducing the THD of load voltage under nonlinear load case (Zhong & Zeng, 2013). The single phase H-bridge insulated gate bipolar transistor (IGBT) inverter circuit along with its control circuitry as shown in Fig.2, is under consideration for designing the capacitive output impedance. The inverter is connected to the AC bus through a switch where load is assumed to be connected (Zhong, 2011). The current $i$ through filter inductor can be passed through integrator block to shape the output impedance capacitive in nature (Zhong & Zeng, 2011). Thus, the feedback path of this closed loop system is shown in Fig.3.

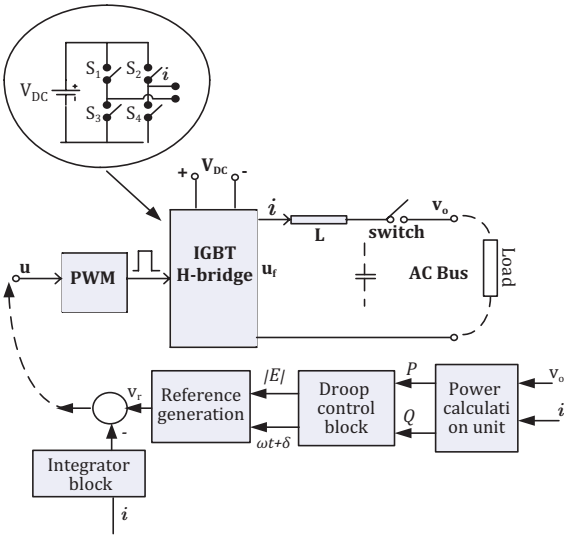



**Figure 2** Physical implementation of single phase inverter

By referring Fig.2 and Fig.3, the following relationships are described in (10).

$$u_f = sL\, i + v_o$$

and

$$u = v_r - \frac{1}{sC_0}\, i \quad (10)$$

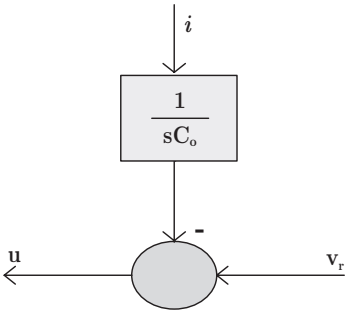



**Figure 3** Controller for achieving capacitive output impedance

Equating both terms of (10) yields

$$v_o = v_r - i\, Z_o(s) \quad (11)$$

Where,

$$Z_o\left(s\right) = sL + \frac{1}{sC_0}$$

$$Z_o\left(s\right) \approx \frac{1}{sC_0} \quad \text{(If } C_0 \text{ is small enough)} \quad (12)$$

The $Z_0$ at the fundamental frequency *(h =1)* can be shaped almost entirely capacitive if the capacitance $C_0$ is small enough to negate the effect of an inductor.

### *A.1 Analytical design process*

As stated earlier, the THD of the voltage is governed by inverter $Z_0$ at harmonic frequencies ($\omega_h$). The procedure of designing $C_0$ or integrator constant is described below (Zhong & Zeng, 2013; Zhong & Zeng, 2011).

The output impedance at harmonic frequency $(h\omega^*)$ is stated in (13).

$$\left|Z_o\left(jh\omega^*\right)\right| = \left|\left(h\omega^* L - \frac{1}{h\omega^* C_0}\right)\right| \quad (13)$$

$h$ and $\omega^*$ are harmonic order and fundamental frequency respectively. Minimization of the following expression, shown in (14) ensures improved THD for a particular virtual capacitor $C_o$.

$$\min_{C_0} \sum_{h=2}^{\infty} i_{1h}^2 \left|Z_o\left(jh\omega^*\right)\right|^2 \quad (14)$$

Where $i_1 h = I_h/I_1$, $h^{th}$ order normalized harmonic current with respect to the fundamental current. Differentiating (14) with respect to $C_o$ and equating to zero yields the optimum capacitance. Therefore, the optimal capacitance is shown in (15).

$$C_0 = \frac{1}{\left(\omega^*\right)^2}\frac{1}{L}\frac{\sum_{h=2}^{N}\frac{i_{1h}^2}{h^2}}{\sum_{h=2}^{N} i_{1h}^2} \quad (15)$$

It is applicable to any a priori estimated harmonic distribution of current. Where $i_{1h}$ is the normalized $h^{th}$ harmonic current.

$$f(C_0) = \left(L\omega^*\right)^2 \sum_{h=2}^{N} i_{1h}^2 \left(h - \frac{1}{h}\frac{\sum_{h=2}^{N} i_{1h}^2}{\sum_{h=2}^{N}\frac{i_{1h}^2}{h^2}}\right)^2 \quad (16)$$

It is evident from the above equation that THD is proportional to the inductance L. A small value of L not only reduces the inductor size and cost but also it enables small integrator gain to ensure the stability of the current loop. Assuming odd harmonics ($h$ = 3,5,7…) are equally distributed, (15) will have the form-

$$C_0 = \frac{1}{\left(\omega^*\right)^2}\frac{1}{L}\frac{\sum_{h=3,5,7\ldots N}^{N}\frac{1}{h^2}}{\sum_{h=3,5,7\ldots N}^{N} 1} \quad (17)$$

Assuming the 3rd and 5th harmonic components, the optimal capacitance from (17) is given by

$$C_0 = \frac{17}{225\left(\omega^*\right)^2 L} \quad (18)$$

The optimal capacitance and $Z_0$ at fundamental frequency are listed in Table 2 for different harmonic frequency numbers. The proposed method enables the first order design of an integrator for different harmonic frequencies. Though, it is possible to build a topology of an integrator with higher order, that is discussed separately in section-III D.

The droop characteristics (corresponding droop control block shown in Fig.2) of capacitive inverter can be obtained by putting θ = -90° in the power flow equations as shown in (19) and (20).

$$P = \left(\frac{EV_o}{Z_o}\left(cos\delta\right) - \frac{V_o^2}{Z_o}\right)\left(cos\theta\right) + \frac{EV_o}{Z_o}\left(sin\delta\right)\left(sin\theta\right) \quad (19)$$

$$Q = \left(\frac{EV_o}{Z_o}\left(cos\delta\right) - \frac{V_o^2}{Z_o}\right)\left(sin\theta\right) - \frac{EV_o}{Z_o}\left(sin\delta\right)\left(cos\theta\right) \quad (20)$$

For capacitive output impedance, θ = -90°

$$P_i = -\frac{E_i V_o}{Z_o} sin\left(\delta\right) \quad (21)$$

$$Q_i = -\frac{E_i V_o}{Z_o} cos\left(\delta\right) + \frac{V_o^2}{Z_o} \quad (22)$$

For very small angle δ,

$$P_i \sim -\delta \;\&\; Q_i \sim -E \quad (23)$$

$$E_i = E^* + n_{iC} Q_i \quad (24)$$

$$\omega_i = \omega^* + m_{iC} P_i \quad (25)$$

The droop characteristics corresponding to (24) and (25) is shown in Fig.4 (i). Where suffix $i$ =1,2 (number of inverters operating in parallel). The parallel operation of inverters becomes important when it comes to availability of high current power electronic devices, system redundancy, reliability expected by critical customers etc. The robust droop control scheme is shown in Fig.4 (ii) (Bhambri et al., 2025).

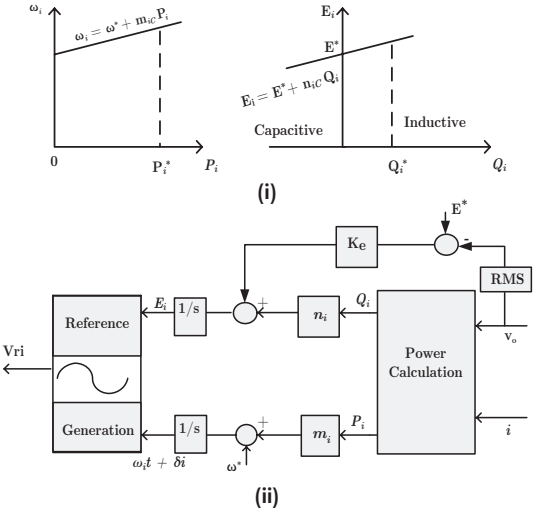



**Figure 4** (i) Droop characteristics (ii) Robust droop control scheme

The $m_{ic}$ and $n_{ic}$ for capacitive inverters are calculated from frequency drop $\left(\frac{m_i P_i}{\omega^*}\right)$ and voltage boost ratio $\left(\frac{n_i Q_i}{E^* K_e} E^*\right)$ which are taken as 1% and 10 % respectively. The amplifier gain ($K_e$) is chosen as 20 (Zhong & Zeng, 2013)

**Table 2** Optimal capacitance and output impedance ($Z_0$)

| Harmonic number | Optimal capacitance | $Z_0$ at fundamental frequency |
|---|---|---|
| 3rd and 5th | 325 μF | -j12.2 $\omega^* L$ (capacitive) |
| 3rd only | 479 μ F | -j8L $\omega^* L$ (capacitive) |
| 5th only | 172.64 μ F | -j24L $\omega^* L$ (capacitive) |

### *B. Bypassing Harmonic current components strategy*

With the exception of capacitive inverters, when the load is nonlinear, the THD of output voltage is significant. The strategy of bypassing harmonic current components, shown in Fig. 5 can be employed to improve the quality of output voltage. Generally speaking, nonlinear loads or/and pulse width modulation cause harmonics in the current $i$ (shown in Fig. 2), which is cause of harmonic voltage drops in the $Z_0$(Zhong, 2011). The output voltage quality degrades and causes high THD due to appearance of harmonic voltage drops on the $Z_0$. Therefore, rather than its type, the output impedance value has a significant impact on voltage THD.

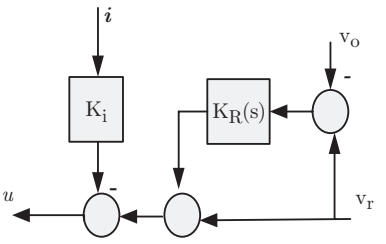



**Figure 5** Controller for improvement in voltage THD

Output impedance ($Z_0$) and $K_R(S)$ are expressed in (26) and (27) respectively (Zhong & Hornik, 2012a; Zhong & Zeng, 2016).

$$Z_o(s) = \frac{sL+K_i}{1+K_R(s)} \quad (26)$$

$$K_R(s) = \sum_{h=3,5,7} \frac{2\xi h\omega s}{(h\omega)^2+2\xi h\omega s+s^2} K_h \quad (27)$$

The $K_R(s)$ is designed to have low gain at low frequency and high gain at high frequency to meet the requirements of power sharing and low output voltage THD. This concept can be applied to all types of inverters. The following set of equations are written for Fig.5.

$$u = v_r - K_i i + K_R(s)(v_r - v_o) \quad (28)$$

$$u = v_r + K_R(s)v_r - K_i i - v_o K_R(s) \quad (29)$$

$$u = v_r(1 + K_R(s)) - (v_o K_R(s) + K_i i) \quad (30)$$

$$u = v_r(1 + K_R(s)) - K_i i_L \quad (31)$$

Where $i_L = i + \frac{K_R(s)}{K_i} v_o$

The current $i_L$ acts as a feedback current $\left(i_L = i + \frac{K_R(s)}{K_i} v_o\right)$, shown in controller block of Fig.6, which is summation of $i$ and current through admittance branch, connected across output terminals. In other words, it can be inferred that the block diagram shown in Fig.5 is equivalent to controller block shown in Fig.6. After careful investigation, it can be seen that structurally the principle is same as that of proportional current feedback control to achieve resistive type inverter with an exception of additional current component of $\left(\frac{K_R(s)}{K_i} v_o\right)$ in an inductor current $i_L$. Filter capacitor (C) and admittance branch $\frac{K_R(s)}{K_i}$ form parallel connection. In simple words, controller block diagram of Fig.2 is equivalent of adding the admittance branch $\left(\frac{K_R(s)}{K_i}\right)$ with the filter capacitor as shown in Fig.7 (i).

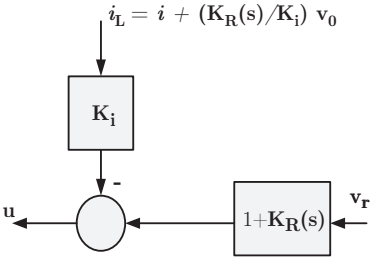



**Figure 6** Equivalent block diagram

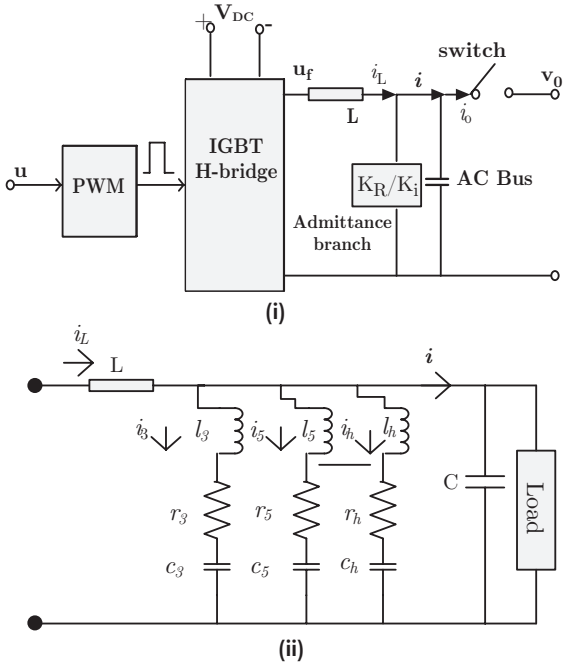



**Figure 7** (i) Equivalent circuit (ii) Individual harmonic currents through admittance branches

$$\frac{\mathrm{K_R(s)}}{\mathrm{K_i}} = \sum_{h=3,5\ldots} \frac{2\xi h\omega s}{s^2+2\xi h\omega s+(h\omega)^2}\frac{\mathrm{K_h}}{\mathrm{K_i}} \tag{32}$$

$$\frac{2\xi h\omega s}{s^2+2\xi h\omega s+(h\omega)^2}\frac{K_h}{K_i} = \frac{1}{\frac{sK_i}{2\xi h\omega K_h}+\frac{K_i}{K_h}+\frac{K_i h\omega}{K_h 2\xi s}} \tag{33}$$

There are parallel admittance branches corresponding to each harmonic frequency component. For example if only two harmonic frequency components $h$ = 3 and 5 are considered then there will be parallel combination of two admittance branches in the equivalent circuit diagram. Each branch is series combination of resistance $\frac{\mathrm{K}_i}{\mathrm{K_h}}$, inductance $\frac{K_i}{2\xi h\omega K_h}$ and capacitance $\frac{2\xi K_h}{h\omega K_i}$, that resonates at the $h^{th}$ harmonic frequency i.e $h\omega$. This is illustrated in Fig.7 (ii).

Where $r_h = \frac{\mathrm{K}_i}{\mathrm{K}_h}$, $c_h = \frac{2\xi \mathrm{K}_h}{h\omega \mathrm{K}_i}$, $l_h = \frac{\mathrm{K_i}}{2\xi h\omega \mathrm{K}_h}$

It is worthwhile to note that, $\frac{\mathrm{K}_i}{\mathrm{K}_h}$ is the remaining impedance (referring (33)) at the $h^{th}$ harmonic frequency. For completely eliminating the $h^{th}$ harmonic voltage component in the output voltage, $\mathrm{K}_i$ should be zero because $\mathrm{K_h}$ is finite. This means that resistive output impedance of an inverter adds the harmonics in the output voltage. It is possible to reduce some harmonic voltage components through trade-off when determining $\mathrm{K}_i$.

### *B.1 Proposed Modification*

In order to further improve the output voltage quality, the strategy discussed in the previous section is modified. The strategy consists of multiple parallel admittances branches (each branch is a parallel combination) tuned to individual harmonic frequency components ($h$ = 3, 5, 7….etc) as shown in Fig. 8.

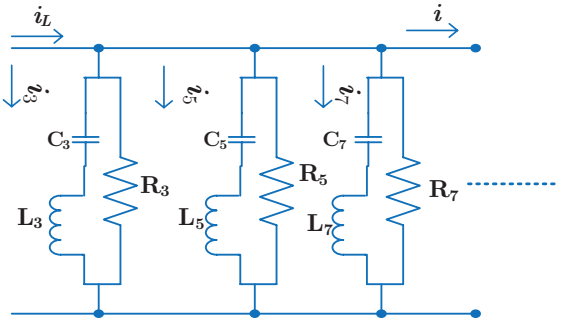



**Figure 8** Shunt resonant filters in proposed modification

Where $\boldsymbol{i_L}$ is filter inductor current, $i$ is output current and $\boldsymbol{i_h}$ ($h = 3, 5,7..$) is bypassed harmonic component of current in $\boldsymbol{i_L}$. The $\boldsymbol{i_h}$ is expressed as follows

$$i_h = \mathrm{v}_o Y_h \quad (h = 3, 5, 7\ldots) \tag{34}$$

Where $Y_h$ is the admittance of $h^{\text{th}}$ circuit, expressed in (35).

$$Y_h = \frac{L_h C_h s^2+1+R_h C_h s}{R_h(L_h C_h s^2+1)} \tag{35}$$

The resonant frequency of circuit tuned at $h^{\text{th}}$ harmonic frequency is,

$$\omega_h = \frac{1}{h\sqrt{L_h C_h}} \tag{36}$$

Now, the inductor current $\boldsymbol{i_L}$ is expressed as

$$i_L = i + \mathrm{v_o}\sum_{\mathrm{h}=3,5,7\ldots}\left(\frac{1}{\mathrm{Y_h}}\right) \tag{37}$$

It is observed through (35), that circuit tuned at $h^{\text{th}}$ harmonic frequency offers infinite addmittance path to the corresponding harmonic frequency current component thereby bypassing it. In this way, the output voltage quality improves when harmonic current components bypass through tuned parallel circuits. An another way to look over this improvement is in terms of output impedance of inverter, which is derived as follows.

The following KVL equation can be written for the filter circuit of an inverter.

$$\mathrm{u} = \mathrm{sL}\, i_L + \mathrm{v_o} \tag{38}$$

L is filter inductor in unit of henry; $i_L$ is current through it and $\mathrm{v_o}$ is the output voltage.

The signal u, generated through the control strategy is expressed as

$$\mathrm{u} = \mathrm{E_r} - \mathrm{K}_i\, i + \mathrm{Y_r(s)}(\mathrm{E_r} - \mathrm{v_o}) \tag{39}$$

Where $\mathrm{K}_i$ is the virtual resistance; $\mathrm{Y_r}$ is virtual resonant admittance function; $\mathrm{E_r}$ is the reference voltage generated in the control scheme.

Upon equating signals in (38) and (39),

$$\mathrm{E_r} - \mathrm{K}_i i + \mathrm{Y_r(s)}(\mathrm{E_r} - \mathrm{v_o}) = \mathrm{sL}\, i_\mathrm{L} + \mathrm{v_o}$$

$$\mathrm{v_o} = \mathrm{E_r} - \frac{\mathrm{sL}+\mathrm{K_i}}{1+\mathrm{Y_r(s)}}\ i_L \tag{40}$$

The output impedance is expressed in (41).

$$\mathrm{Z_o} = \frac{\mathrm{sL}+\mathrm{K_i}}{1+\mathrm{Y_r(s)}} \tag{41}$$

The magnitude and phase plots of $Z_o$ are shown in Fig.9.

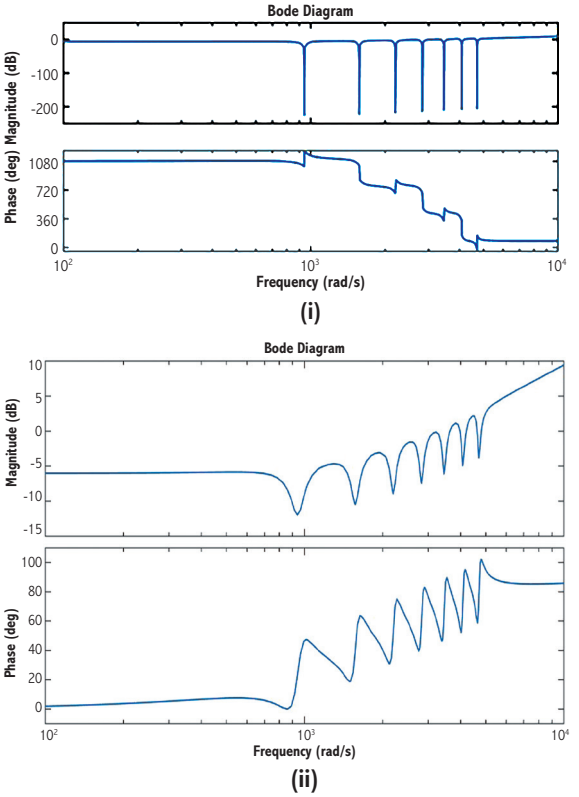



**Figure 9** Magnitude and phase plot of $Z_o$
(i) with $r_{par} = 0$ (ii) with $r_{par} = 0.1\ \Omega$

The magnitude plot, shown in Fig.9 (i) reveals that output impedance of inverter at dominating harmonic frequencies ($h$ = 3, 5 ,7, 9, 11, 13, 15) is close to zero. Therefore, voltage drop at these harmonic frequencies also tend to zero thereby improving the quality of the output voltage. By carefully examining (35), it is observed that phase value nearby these frequencies may not acquire zero value if parameters are not tuned properly, leading to instability in the system. In order to overcome this, a small parasitic resistance $r_{par}$ ( $\approx 0.1\ \Omega$) is considered in series with $L_h$.

With this consideration, the magnitude and phase plots are shown in Fig.9 (ii) and the admittance at $h^{\text{th}}$ harmonic frequency is $\frac{R_h + r_{par}}{r_{par}\, R_h}$.

### *C. Harmonic droop control*

The superposition theorem allows for separate analysis of a circuit's (linear in nature) supply and sink at distinct frequencies. This concept will be exploited to analyze harmonic behavior in the inverter systems. The mathematical model for an inverter connected to grid/load, or both is shown in Fig.10 (i). The inverter is modeled as a voltage reference ($\mathrm{v_r}$) with $\mathrm{Z_0}$, while the load is modeled as a combination of current and voltage sources. The output or terminal voltage is stated in (42) followed by its fundamental and $h^{th}$ harmonic component (Zhong & Hornik, 2012a).

$$\mathrm{v_o} = \mathrm{v_{o1}} + \textstyle\sum_{\mathrm{h=2}}^{\infty} \mathrm{v_{oh}} \tag{42}$$

$$\mathrm{v_{o1}} = \sqrt{2}\, \mathrm{V_{o1}} \sin\left(\omega^* t\right) \tag{43}$$

and,
$$\mathrm{v_{oh}} = \sqrt{2}\, \mathrm{V}_{oh}\ \sin\left(h\omega^* t + \psi_h\right) \tag{44}$$

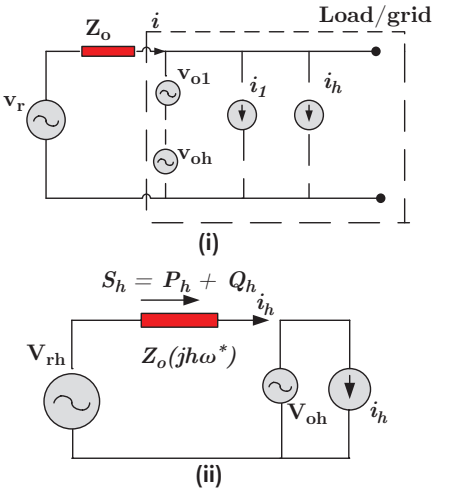



**Figure 10** (i) Circuit including $h^{\text{th}}$ harmonic component
(ii) $h^{\text{th}}$ harmonic circuit

In this equation, $\omega^*$ represents the system's rated fundamental angular frequency, $v_{01}$ represents the fundamental component's rms voltage, and $v_{oh}$ represents the harmonic component's rms voltage. The output or load current is described in (45).

$$i = \sum_{h=1}^{\infty} i_h \tag{45}$$

$$i_h = \sqrt{2}\, I_h \sin\left(h\omega^* t + \varphi_h\right) \tag{46}$$

Nonlinear loads or harmonic currents cause zero current to flow through voltage sources connected in series. In general, the voltage reference $v_r$ can be stated as,

$$v_r = \sum_{h=2}^{\infty} v_{rh} + v_{r1} \tag{47}$$

$$v_{r1} = \sqrt{2}\, E \sin\left(\omega^* t + \delta\right) \tag{48}$$

$$\text{and,}\quad v_{rh} = \sqrt{2}\, E_h \sin\left(h\omega^* t + \delta_h\right) \tag{49}$$

Inverters with droop controllers frequently set $E_h$ to zero. This study will use nonzero $E_h$ to reduce $v_{oh}$ to near-zero values. To analyze this circuit, decompose it into number of circuits at each harmonic frequency using the superposition theorem. Fig.10 (ii) depicts the system's $h^{th}$-harmonic circuit.

The load of the circuit $(V_{o1}/I_1)\angle -\varphi_1$ at the fundamental frequency is calculated by combining the voltage source $V_{o1}\angle 0^o$ and the current source $I_1\angle\varphi_1$. If $v_{oh}\ (h=1)$ is close to zero, the right-hand side of Fig.10 (ii) shows a current source ($i_h$). An inverter (also known as a generator) supplies actual and reactive power to a load at the appropriate voltage and frequency, as determined by industry standards and/or laws. Specifically, this should be performed at the fundamental frequency with no inclusion of harmonics (Wakileh, 2001). When numerous inverters are linked in conjunction, they should distribute reactive and real power in ratio of their capacities (Zhong, 2011; Zhong & Zeng, 2016). So, what occurs with harmonics? The output voltage should have zero harmonics, $v_{oh}$ = 0 (h = 2,3,...), even if there are harmonics in the current *(i)*. To achieve this, the voltage drop of the $h^{th}$-harmonic current $\sqrt{2}\, I_h \sin(h\omega^* t + \varphi_h)$ on the output impedance $Z_o(j\omega)$ must be equal to the $h^{th}$-harmonic component of the voltage reference $\sqrt{2}E_h \sin(h\omega^* t + \delta h)$, where $E_h = I_h|Z_o(jh\omega^*)|$ and $\delta_h = \varphi_h + \angle Z_o(jh\omega^*)$. This idea is exploited to design a control system that reduces harmonics in the output voltage.

### *C.1 Power delivery to a current source*

In Fig. 11, a voltage source ($v_r$) delivers power to a current source ($I\angle 0^o$) via an impedance ($Z_o\angle\theta^o$). Finally, the terminal voltage is,

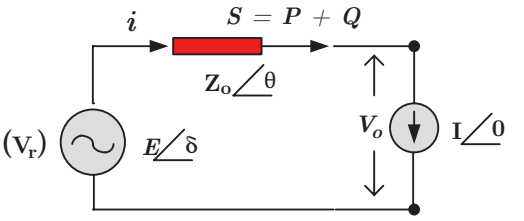



**Figure 11** Power deliver to a current source by voltage source

$$V_o = E\angle\delta - Z_o I\angle\theta \tag{50}$$

$$V_o = E\cos\delta + j\,E\sin\delta - Z_o(I\,\cos\theta\, +\, j\,I\sin\theta) \tag{51}$$

The reactive and active powers delivered to terminal are,

$$Q = E\,I\,\delta - Z_o I^2\,\sin\theta \tag{52}$$

$$P = E\,I - Z_o I^2\,\cos\theta \tag{53}$$

$Q \sim \delta$ , $P \sim E$ (for any $Z_o\angle\theta$ type). This differs from the situation of power deliver to voltage source, where these relations alter depending on the nature of impedance. The usual droop approach therefore takes the form of (54) and (55).

$$E_i = E^* - P_i n_i \tag{54}$$

$$\omega_i = \omega^* - Q_i m_i \tag{55}$$

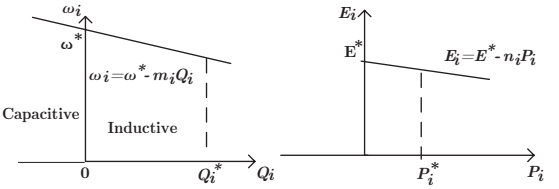



**Figure 12** Droop characteristics for inverters maintaining constant o/p current (for any impedance type)

The characteristics in (54) and (55) are drawn in Fig.12. Further, in order to ensure that $P$-$E$ and $Q$-$\omega$ terms are of negative (-) feedback, so that droop control is able to adjust the voltage and frequency, the signs before $P_i n_i$ and $Q_i m_i$ are all negative (-) that makes them droop terms (Zhong & Hornik, 2012a).

The harmonic voltage source ($v_{oh}$), as shown in Fig.10 (i), must be zero in order to compel the $h^{th}$ harmonic components in an inverter's output voltage

to be (almost) zero. Stated otherwise, there should be zero real and reactive powers supplied to the current source $i_h$ in Fig. 10 (ii). Therefore, for the $h^{th}$ harmonic components $(h \neq 1)$, the voltage set-point $E^*$ for the droop control acquired in (54) should be zero. Additionally, the $h^{th}$ -harmonic frequency set-point in (55) should be the $h^{th}$-harmonic frequency. Consequently, the $h^{th}$ -harmonic droop controller is as follows.

$$E_h = -n_h P_h \tag{56}$$

$$\omega_h = h\omega^* - Q_h m_h \tag{57}$$

where $m_h$ and $n_h$ are the appropriate droop coefficients, and $P_h$ and $Q_h$ are the active and reactive powers at the terminal for the $h^{th}$-harmonic frequency, respectively. Here, the $h^{th}$ harmonics are reflected by changing the subscripts of the pertinent variables. The $E_h$ (rms value) and the phase angle produced by an integration of $\omega_h$ can then be used to establish the reference voltage $\mathrm{v_{rh}}$ the $h^{th}$-harmonic frequency. In actuality, a harmonic frequency $\omega_h$ can be obtained from $h\omega t$ by adding $\delta h$, which is integrated from $-Q_h m_h$, rather than creating it from (57). The phase of voltage reference at the fundamental frequency is denoted by $\omega t$. This results in Fig.13, suggested as $h^{th}$ harmonic droop controller.

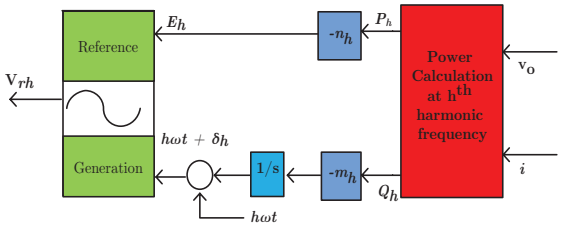



**Figure 13** $h^{th}$ harmonic droop controller [4]

The $\mathrm{v_{oh}}$ can be approximated as,

$$V_{oh} = E_h - Z_o(j\omega^* h) I_h = -n_h V_{oh} I_h - Z_o(j\omega^* h) I_h \tag{58}$$

$$V_{oh} = -\frac{Z_o(j\omega^* h) I_h}{1 + n_h I_h} \tag{59}$$

Its endowment to the THD is $\frac{Z_o(j\omega^* h) I_h}{E^*(1+n_h I_h)}$. In order to reduce THD of the output voltage, $Z_o$ at harmonic frequencies should be reduced. Also the parameter $n_h$ must be chosen to be high to make $V_{oh}$ small as long as the system is stable. The parameter $m_h$ is chosen in a similar way as $m_1$ because $\frac{m_h Q_h^*}{\omega^* h}$ is the drop at the $h^{th}$ harmonic frequency and that is same as that of the drop at the fundamental frequency, $\frac{m_1 Q^*}{\omega^*}$. Therefore,

$$m_h = m_1 \frac{hQ^*}{Q_h^*} \tag{60}$$

In this paper, third and fifth harmonic droop controllers are adopted with $m_h$ = 50 and $n_h$ = 5 respectively. The droop coefficients ($m_i$, $n_i$, $i$ = 1,2) at the fundamental frequency and amplifier gain ($K_e$) are taken same as that of capacitive inverter. The virtual resistance ($K_i$, $i$ = 1,2) for two inverters are chosen as 2 and 4 respectively as resistive droop characteristics is adopted for this strategy (Zhong, 2011; Zhong & Hornik, 2012a; Bhambri, Kumawat, et al., 2023).

To generate the necessary $\Sigma \mathrm{v_{rh}}$, the controller can incorporate several harmonic droop controllers that correspond to the harmonic orders, therefore reducing multiple harmonics in the output voltage. The $\mathrm{v_r}$, voltage reference is then produced by the droop control at the fundamental frequency ($h$ = 1) and may be derived by adding $\Sigma \mathrm{v_{rh}}$ to $\mathrm{v_{r1}}$. The complete scheme is shown in Fig.14.

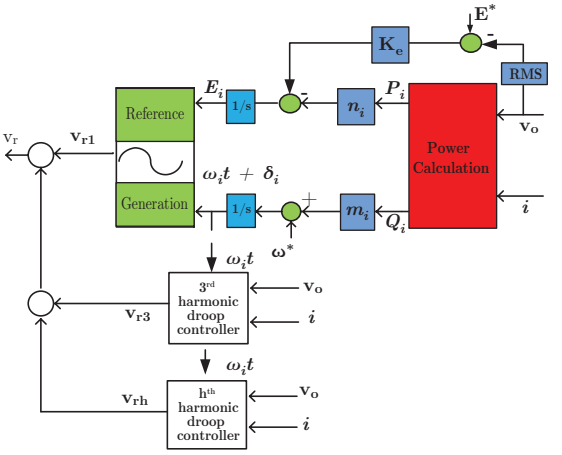



**Figure 14** Complete scheme of $h^{th}$ harmonic droop controller

### *D. Resonant Impedance Topology*

RI topology, which stands for resonant impedance is shown in Fig. 15. It is an extension of integral controller, described in section A.1. Level-1 corresponds to the first order design which can address up to one harmonic frequency of interest. In the same way, $h_n$ level topology can address up to $h_n$ harmonic frequencies ($h$ = 3,5,7….$h_n$) simultaneously. The various parameters of this topology are designed through procedure given below (Zhong, 2011; Zhong & Hornik; 2012a, Cheepati et al., 2025).

### *D.1 Level-2 design*

When two levels of RI are considered, the equivalent virtual impedance is computed as,

$$\mathrm{Z_v(s)} = \frac{1}{sC_1} \cdot \left(\frac{1}{sC_2} + \mathrm{s}L_2\right) / \left(\frac{1}{sC_1} + \left(\frac{1}{sC_2} + \mathrm{s}L_2\right)\right) \quad (61)$$

$$\mathrm{Z_v(s)} = \frac{\frac{1}{sC_1} \cdot \left(\frac{1}{sC_2} + sL_2\right)}{\left(\frac{1}{sC_1} + \left(\frac{1}{sC_2} + sL_2\right)\right)}, \quad (62)$$

$$\mathrm{Z_v(s)} = \frac{s^2 C_2 L_2 + 1}{s(C_1 + C_2 + C_1 C_2 L_2 s^2)} \quad (63)$$

Considering filter inductor, the output impedance is described in (64).

$$Z_o(\mathrm{s}) = Z_\mathrm{v}(\mathrm{s}) + (\mathrm{s}L) \quad (64)$$

In order to reduce the THD of output voltage, output impedance at dominating harmonic frequencies ($h$ = 3,5,7…) should be zero. The numerator of impedance function $\mathrm{Z_o(s)}$ can be designed to achieve the aforesaid objective.

The numerator of $\mathrm{Z_o(s)}$ is shown in (65).

$$C_1 C_2 \mathrm{L} L_2 \mathrm{s}^4 + \mathrm{s}^2\left(C_2 L_2 + C_2 \mathrm{L} + C_1 \mathrm{L}\right) + 1 = 0 \quad (65)$$

The (65) can be compared with $\left(\mathrm{s}^2 + \omega^2 h_1^2\right)\left(\mathrm{s}^2 + \omega^2 h_2^2\right) = 0$, in order to design the parameters.

$$C_1 C_2 \mathrm{L} L_2 h_1^2 h_2^2 \omega^4 = 1 \quad (66)$$

$$\left(C_2 L_2 + C_2 \mathrm{L} + C_1 \mathrm{L}\right) = \frac{(h_1^2 + h_2^2)}{h_1^2 h_2^2 \omega^2} \quad (67)$$

The (66) and (67) are used to compute either $C_1$ or $C_2$ in terms of L, $L_2$, $h_1$ and $h_2$ subjected to constraint stated in (68).

$$\frac{C_1}{C_2} = \frac{\mathrm{L} + L_2}{\mathrm{L}} \quad (68)$$

For $h_n$ level design, the constraint can be generalized as,

$$\frac{C_1}{C_2} = \frac{L + L_2}{\mathrm{L}} = \cdots \frac{L + L_2 + \ldots L_{h_n}}{\mathrm{L}} \quad (69)$$

Upon observing (65), it is evident that virtual impedance function has resonant peaks which in general, can be controlled by adding resistor $\mathrm{R_V}$ in parallel with $C_{h_n}$. An alternative way to reduce these peaks is to add $\mathrm{r_{esr}}$ (equivalent series resistance) in series with filter capacitor. The value of $\mathrm{r_{esr}}$ is considered as 1 Ω while applying this topology.

The magnitude and phase plot of $\mathrm{Z_V(s)}$ for level-2 and level-3 design are shown in Fig.16. The magnitude of output impedance at dominating harmonic frequencies (selected in design procedure), is reduced.

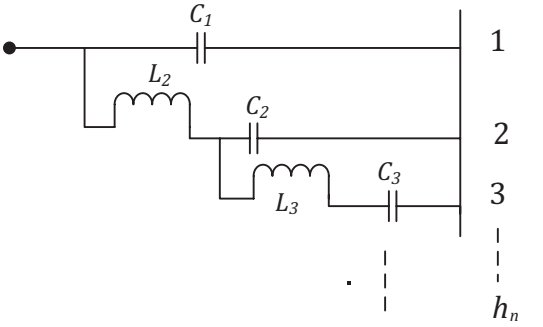



**Figure 15** Resonant impedance topology

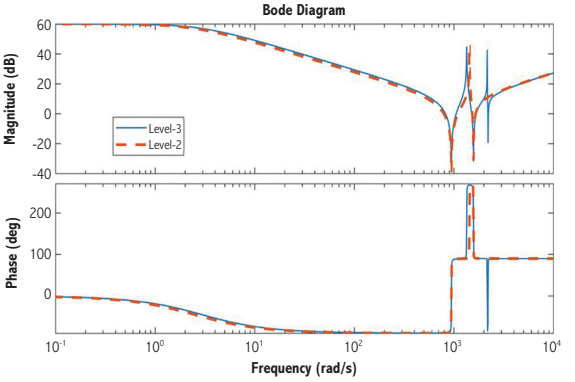



**Figure 16** Magnitude and phase plots of output impedance

## IV. RESULT AND DISCUSSION

***A. Scenario:*** The simulation scenario consists of two single phase inverters (50 VA and 25 VA rating) connected in parallel and feeds a common nonlinear load (full bridge rectifier with LC filter, $\mathrm{L_{NL}}$ = 150μH and $\mathrm{C_{NL}}$= 1000μF, $\mathrm{R_{NL}}$ = 9Ω). The robust droop control model of single phase inverter is used for validating the strategies.The necessary system parameters are shown in Table 3.

***(i) BHCC:*** Initially both inverters share the common load. Inverter-1 is disconnected at *t = 7.5 sec* and inverter 2 shares the load only. THD of the load voltage is reduced to 5% when both inverters are operating and 5.35% when only single inverter is operating as shown in Fig.17. It is observed from the FFT analysis that individual harmonic components, $\mathrm{v_{oh}}$ are reduced below 3%.

The modified BHCC shows superior performance, reducing $\mathrm{THD_V}$ to 2.8% as shown in Fig.18.

***(ii) Capacitive inverter:*** Initially both inverters share the common load. Inverter-1 is disconnected at $t = 4.5\ sec$ and inverter 2 shares the load only. THD of the load voltage is reduced to 15% when both inverters are operating and 20% when only single inverter is operating as shown in Fig.19.

***(iii) HDC:*** Both inverters share the common load. THD of the load voltage is reduced to 9.29% when both inverters are operating as shown in Fig.20.

***(iv) Resonant Impedance Topology:*** Initially both inverters share the common load. Inverter-1 is disconnected at $t = 4.5\ sec$ and then inverter-2 shares the load only. THD of the load voltage is reduced to 9% when both inverters are operating as shown in Fig.21. The performance of different strategies in terms of $THD_V$ is shown in Table 4.

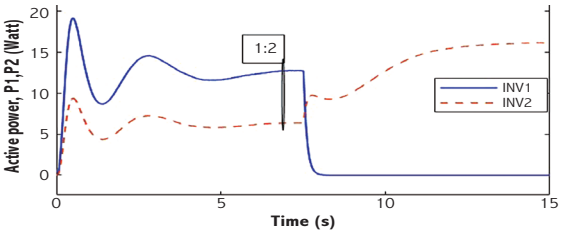
**Table 3** System parameters for BHCC startegy

| Parameters | value | Unit |
|---|---|---|
| $F$ | 50 | $Hz$ |
| $VDC$ | 42 | $V$ |
| $E^*$ | 12 | $V$ |
| $f_s$ | 7500 | $Hz$ |
| L*(inverter)* | 2.35 | $mH$ |
| $\omega^*$ | 314 | $rad/s$ |
| C *(filter)* | 22 | $\mu F$ |
| $v$ | 10 | |
| $m_1$ | 0.1 | $rad/Var$ |
| $m_2$ | 0.2 | $rad/Var$ |
| $n_1$ | 0.4 | $V/W$ |
| $n_2$ | 0.8 | $V/W$ |
| $K_1$ | 2 | |
| $K_2$ | 4 | |
| $\xi$ | 0.01 | |
| $K_9$ | 1 | |
| $K_7$ | 2.5 | |
| $K_5$ | 10 | |
| $K_3$ | 14 | |

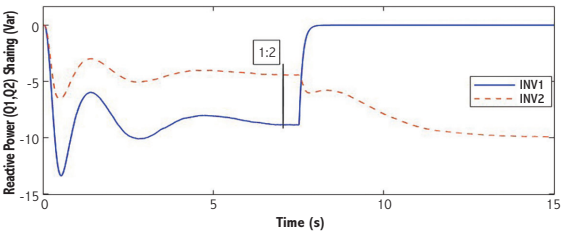
*Note.* Adapted from "Parallel Operation of Inverters," in *Control Of Power Inverters In Renewable Energy And Smart Grid Integration* (pp. 297–333), by Q. C. Zhong and T. Hornik, 2012, Wiley-IEEE Press.

**Table 4** Performance in terms of $THD_V$

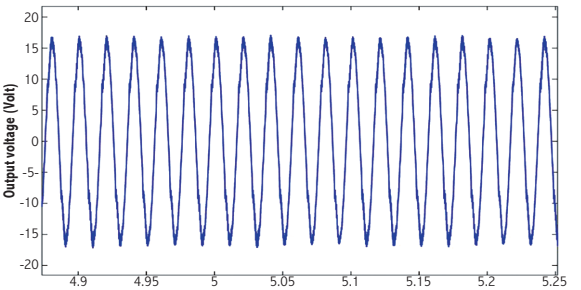
| Operating condition | Strategy | $THD_V$ in % |
|---|---|---|
| 2 single phase inverters operating in parallel | BHCC | 5 |
| | Modified BHCC | 2.8 |
| | Capacitive inverter | 15 |
| | HDC | 9.29 |
| | RI | 9 |



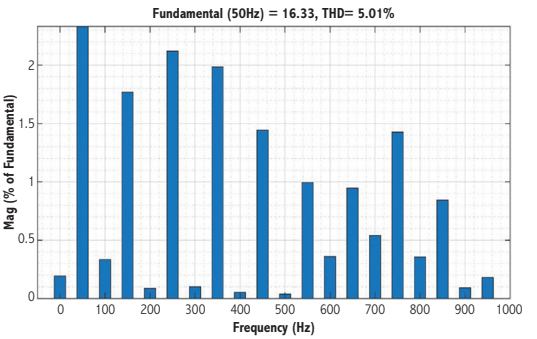
(i)



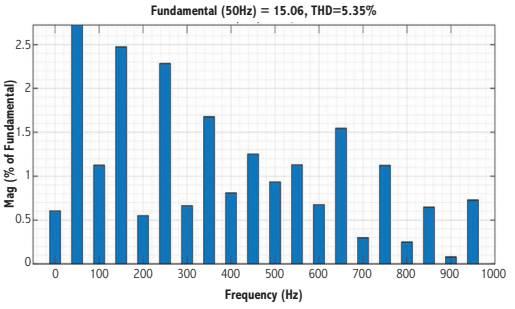
(ii)



(iii)

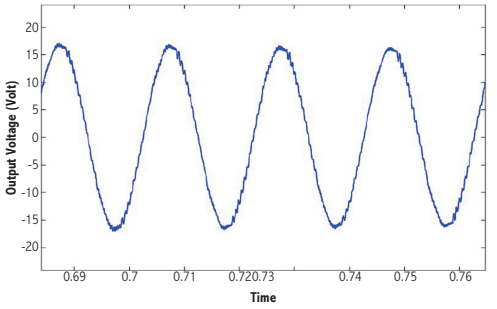


(iv)

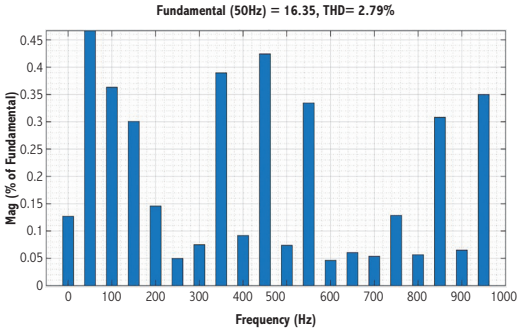



(v)

**Figure 17** BHC strategy (i) active power sharing vs time (ii) reactive power sharing vs time (iii) Load voltage (iv) $THD_V$, when both inverters are operating (v) single inverter is operating.

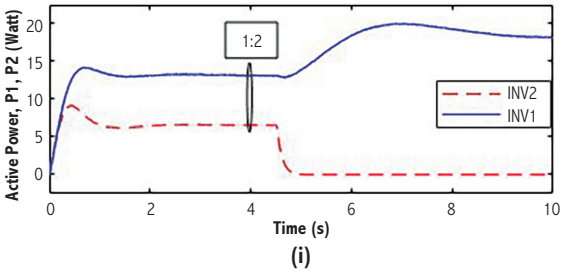



(i)

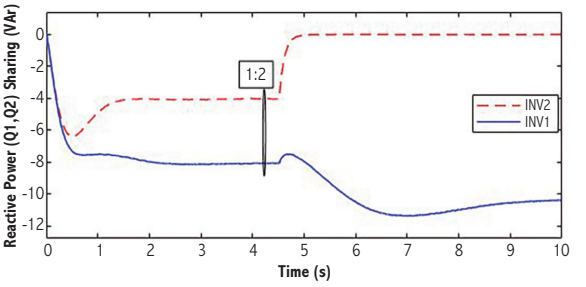



(ii)

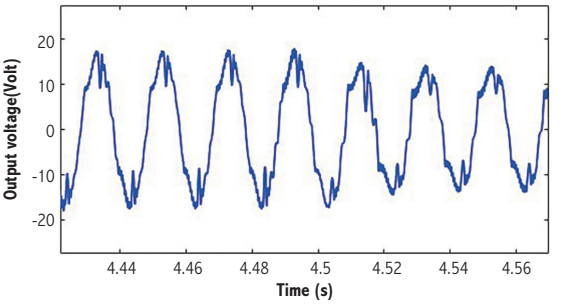
**Figure 18** BHCC strategy with modification (i) output voltage (ii) $THD_V$, when both inverters are operating



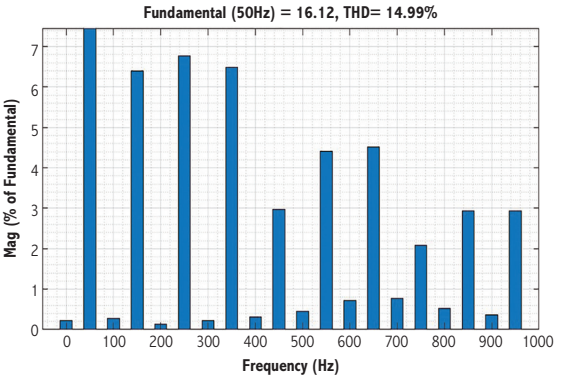

(i)



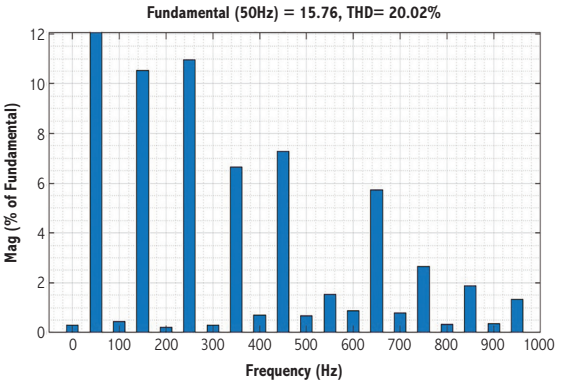

(ii)




(iii)




(iv)




(v)

**Figure 19** Capacitive inverter strategy (i) active power sharing vs time (ii) reactive power sharing vs time (iii) Load voltage vs time (iv) THD, when both inverters are operating (v) single inverter is operating.

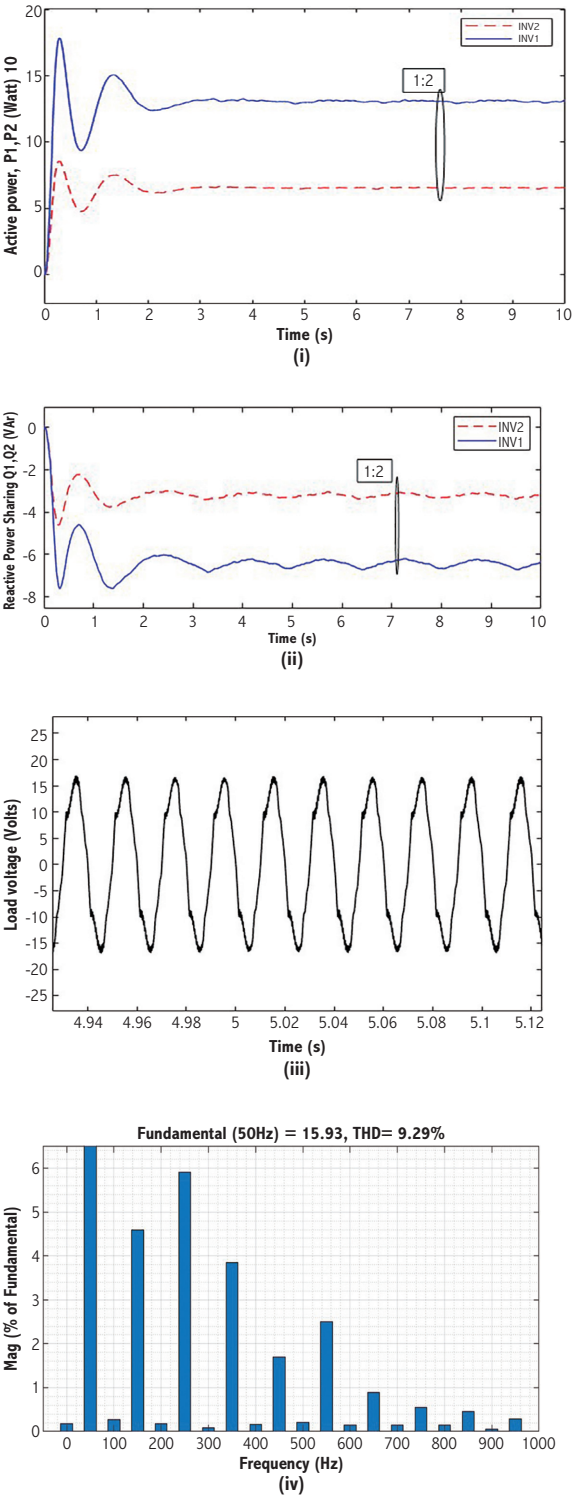



**Figure 20** HDC strategy (i) active power sharing vs time (ii) reactive power sharing vs time (iii) Load voltage vs time (iv) THD when both inverters are operating.

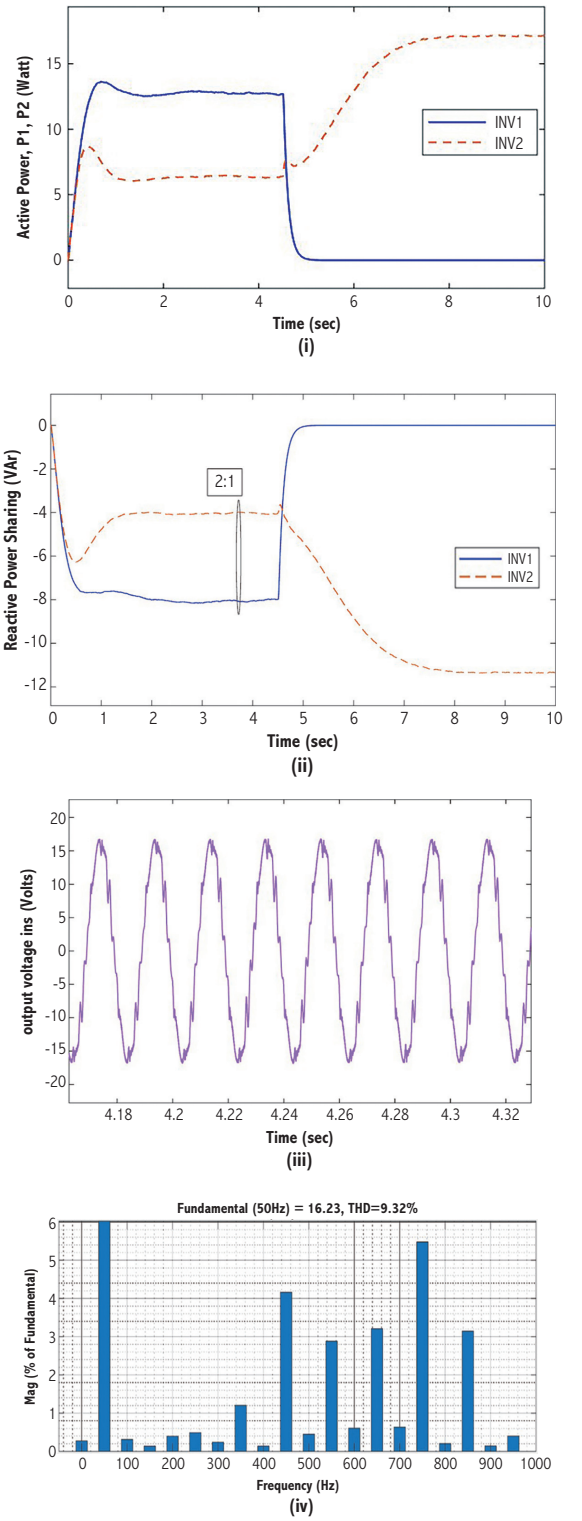



**Figure 21** Resonant impedance strategy (i) active power sharing vs time (ii) reactive power sharing vs time (iii) Load voltage vs time (iv) $\mathrm{THD_V}$, when both inverters are operating.

**Observation:** In each case, the active and reactive power are shared to the load in the ratio of power rating of inverters . As far as THD of the load voltage is concerned, BHCC strategy effectively reduces the $THD_V$ to nearly 5 % followed by 9 % with HDC, 15 % on applying capacitive inverters and approximately 9 % with resonant impedance topology (Level-3 design). The voltage quality is enhanced further by modifying BHCC with recorded $THD_V$ 2.8%. As per revelation of the FFT analysis, with modified control strategy, the individual harmonic components in the output voltage are less than 0.5 % relative to the fundamental.

## V. CONCLUSION

In this paper, the core factors behind output voltage degradation in renewable energy based systems are outlined. Four strategies have been thoroughly described with an objective of improving the output voltage quality under nonlinear load case. The various sources of harmonic components in the output voltage are underlined and a common conclusion is drawn, that is to reduce the output impedance at dominating harmonic frequencies ($3^{rd}$, $5^{th}$, $7^{th}$) for mitigation of $THD_V$. Subsequently, for their comparative evaluation, the FFT analysis is done by using simulation models. Additionally, proportionate power sharing of inverters is demonstrated through robust droop control structures and bypassing components strategy is modified to further improve the voltage quality. In the future work, the discussed strategies would likely to be applied for more practical microgrids consisting of feeder lines between filter and bus with real time simulation.

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